CY3652
USB Development System
User's Guide

Version 1.5

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DOCUMENT HISTORY

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REV	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
1.0	-	10/29/97	TEN	First Alpha Release
1.1	-	10/29/97	TEN	Added to "differences from chip" section
1.2	-	1/5/98	TEN	Changes for Beta Version
1.3	-	1/27/98	TEN	Minor Revisions
1.4	-	4/15/98	TEN	Designator Errors on Downstream Ports
1.5	-	4/17/98	TEN	Modified Figure 4. to reflect changes to Rev. D PCB

1. Overview

The Cypress CY3652 USB Development System is a powerful tool to assist development of user hardware and firmware with emulated Cypress USB ICs. In the full development system environment (Figure 1.), a PC-based interface facilitates debugging through break-traps, single stepping, and display/modification of registers and data RAM. In this mode, firmware can be implemented in on-board EPROM, or downloaded to program RAM. The RAM option provides a quick and easy method for testing firmware revisions.

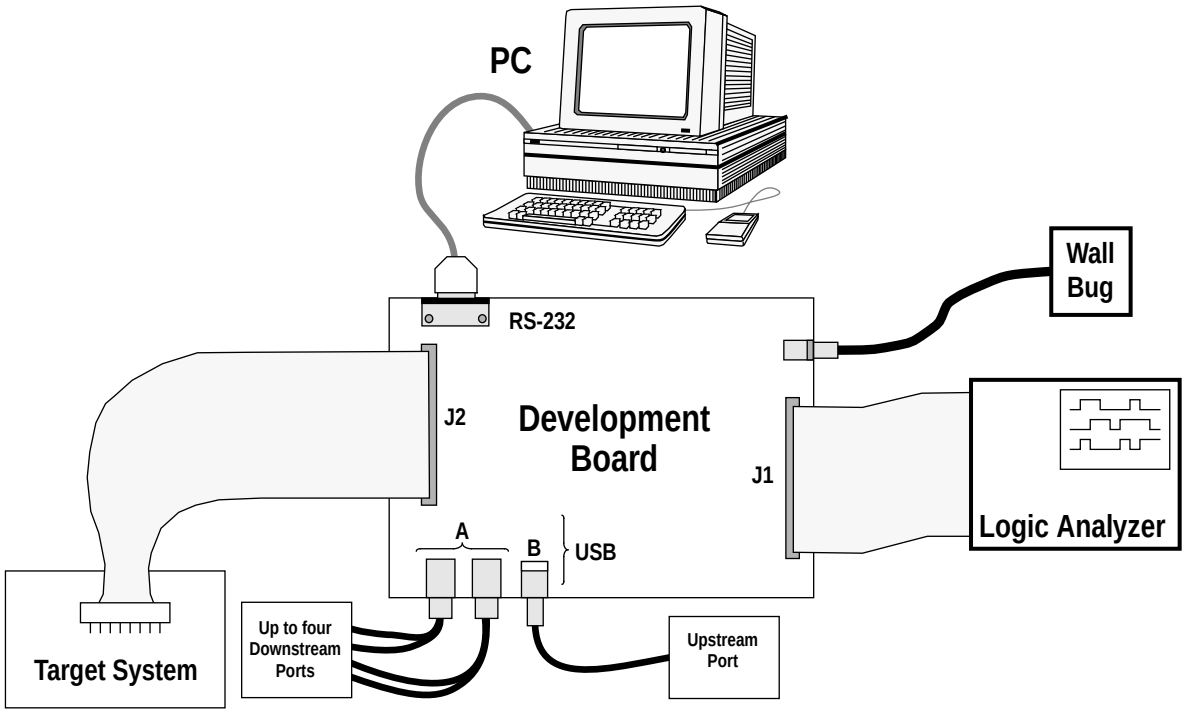


Figure 1. Typical USB Development Environment

Stand-alone mode (Figure 2.) allows portable system operation. In this case, user firmware is loaded in EPROM, and only power need be applied to produce a fully operating emulated USB chip.

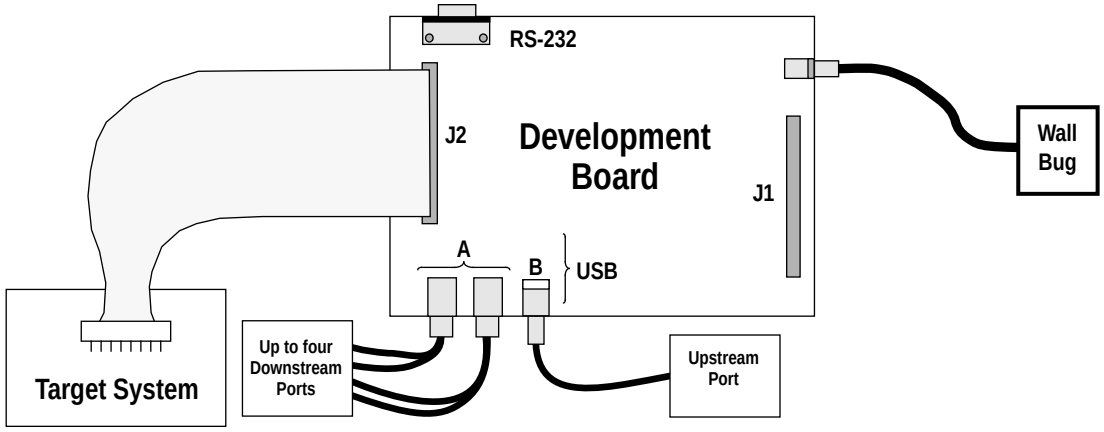


Figure 2. Stand-alone Environment

Figure 3. shows a block diagram of the development board, illustrating the major system components and the user interfaces. The board supports a family of Cypress USB ICs, with varying amounts of on-chip EPROM, RAM, I/O, etc. Consult the individual device specification for details on the IC being emulated.

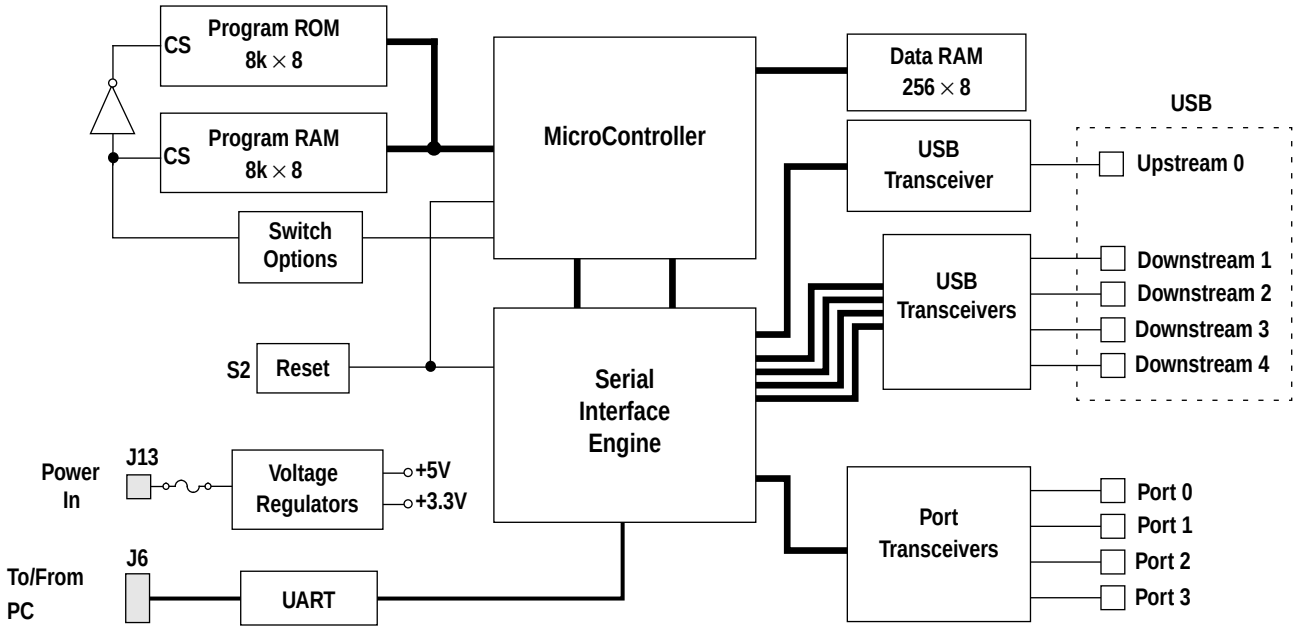


Figure 3. Development Board Functional Block Diagram

2. Kit Contents

The USB Development System contains the following items:

- USB development board
- Wall transformer power supply ("Wall bug"), 6 Volt DC, center negative
- USB cable
- RS-232 9-pin to 9-pin cable
- 9-pin to 25-pin adapter for RS-232 cable
- CY3652 USB Development System User's Guide (this user's guide)
- USB Development System Software Guide
- CYASM Assembler User's Guide
- USB Monitor/Debug Software (3 disks)
- CYASM Assembler software and example application software (1 disk)
- Registration Card

3. Hardware Installation

This section describes the hardware installation steps necessary for operating the development board. These

include supplying power to the board, connecting to a PC, and configuring on-board switches. Refer to Figure 4. for locations of components mentioned in this document; Figure 1. shows typical connections for the system development environment.

3.1. Power Connection

The development board is designed to be powered by the enclosed wall transformer. Connect the transformer to a 110V AC source, and to power jack J10 on the board. +5V and +3.3V are generated by regulators on the board. The green LED will light when power is applied.

Be careful not to accidently short the power from the "wall bug", it has an internal fuse (not accessible) that could blow and render the supply inoperative.

3.2. Jumpers

Jumper JP1, at the lower left corner of Figure 4., applies VDD (+5V) to pin 58 of connector J2. Without JP1, no connection to VDD occurs on J2. The board is shipped with the jumper installed.

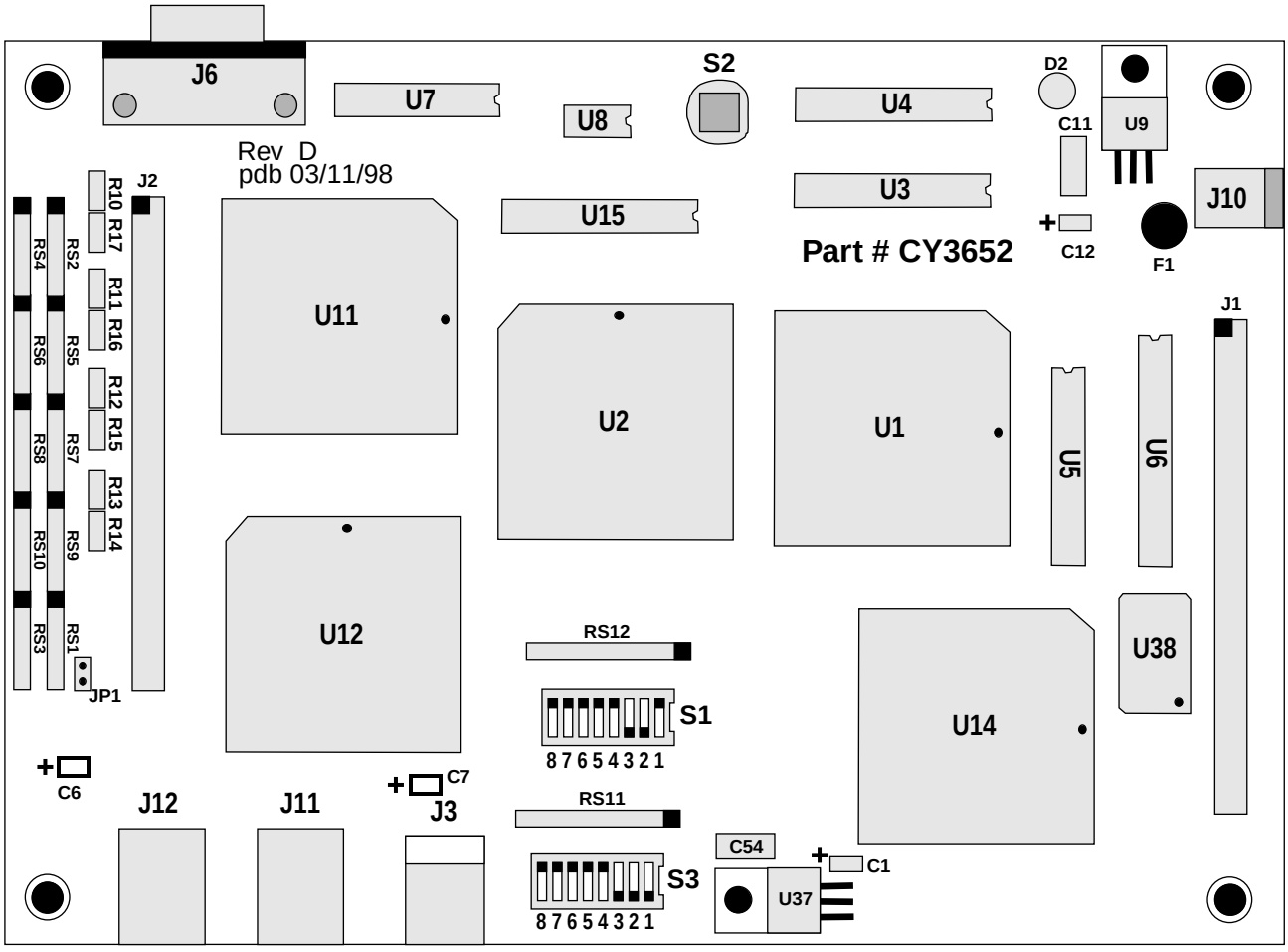


Figure 4. Development Board Layout

3.3. PC Communication

For communicating with a PC, plug the enclosed RS-232 cable into the 9-pin connector J6 on the board. The other end of the cable should be connected to the appropriate COM port on the PC, typically COM1 or COM2, depending on the PC's configuration. A 9-pin to 25-pin adapter is provided in case the PC port uses a 25-pin connector.

The required communication settings for the PC are:

Baud Rate	19200
Data Bits	8
Parity	None
Stop Bits	1
Flow Control	None used

It is also recommended that the UART FIFO size settings be set to the minimum values. Do the following steps in Windows95™ to change the FIFO settings:

- On the desk-top, double click on the "My Computer" Icon and then double click on the "Control Panel" Icon. Alternately, use the "start" menu and choose "Settings" and then "Control Panel".
- In the "Control Panel" window, double click on the "System" Icon.
- In the "System" window click on the "Device Manager" tab. Then scroll down through the list of devices to the serial port used for the USB Development Board, this is usually COM1 or COM2. Select the appropriate device by double clicking.
- This brings up a serial device window, inside you will see tabs, select the "Advanced" tab. This sub-widow contain the settings for the serial transmit and receive FIFOs. Set the receive FIFO to 1 and set the transmit FIFO to 3 if this is a valid setting, otherwise set the FIFO size to 1.

3.4. Switch Settings

Two 8-position DIP switches provide configuration options for the two on-board FPGAs. Table 1 and Table 2 list options for switches S1 and S3 respectively. Further information on these options is given in Section 5. Unused switches should be left in the default setting, as these may support internal test modes.

Table 1: Switch S1 Configuration

Position	Open (1)	Closed (0)	Function
1	Default	–	Unused
2	Enable	Disable	Watch Dog Reset
3	Enable	Disable	USB Bus Reset
4	Default	–	Unused
5	Default	–	Unused
6	Default	–	Unused
7	Default	–	Unused
8	Default	–	Unused

Table 2: Switch S3 Configuration

Position	Open (1)	Closed (0)	Function
1	Program RAM	Program ROM (U5)	User-code Source
2	–	Default	Required
3	–	Default	Required
4	Default	–	Unused
5	Default	–	Unused
6	Default	–	Unused
7	Default	–	Required
8	Default	–	Required

4. Software Installation

For information on operation of the interactive PC debug environment, refer to the USB Development System Software Guide.

For information on the CYASM assembly language programming and the assembler, refer to the CYASM Assembler User's Guide.

5. Operation

5.1. Differences between the chip and the development board

The development board is lacking some of the features that are present on the integrated circuit. Some of the important differences are:

1. No programmable drive strength on DAC port pins
2. I/O Ports do not operate exactly like the chip. See Section 5.4 below.
3. The development board is not bus powered and therefore it is not initialized when the USB connector is first attached.
4. Four of the seven down-stream ports are implemented on the development board.
5. EPROM Programming is performed by removing U5, erasing, re-programming in a standard EPROM programmer and then re-installing into the U5 socket.
6. There is no PLL, the 48 MHz clock is generated on the development board by a crystal oscillator.
7. Data traveling between upstream and downstream ports (both directions) is slower by 1/2 of a bit period.

5.2. Firmware ROM vs. RAM operation

The user's program code will be executed from either a ROM (U5) or program RAM, depending on the setting of switch S3-1 (see Table 2). The U5 ROM is a Cypress CY7C261-45, an 8k × 8 UV-erasable EPROM. The program RAM supports the same memory size as the EPROM.

To program or erase the EPROM, refer to the data sheets for the Cypress CY7C261-45. The part can be repeatedly reprogrammed as user firmware is updated. Follow appropriate ESD precautions when handling the part. When installing U5 in the development board, note the IC orientation guide, shown on the board and in Figure 4.

The following examples illustrate typical procedures for operating from either ROM or RAM.

Example 1: Program ROM Operation

1. Develop assembly code; program this into the U5 Cypress CY7C261-45 EPROM.
2. Remove power from the development board.
3. Install U5 into the development board.
4. Set switch S3-1 for program ROM operation (see Table 2)
5. Apply power to the board.

Example 2. Program RAM Operation

1. Develop assembly code; assemble and create object code file (see CYASM Assembler User's Guide; the object file has a .rom suffix).
2. Set switch S3-1 for program RAM operation.
3. Apply power to the board, and halt microcontroller execution with the "break" command on the PC debug software.
4. Download the user object code file to program RAM (refer to the USB Development System Software Guide).
5. Press the reset switch S2.

Firmware will be held in program RAM until modified via the PC interface, or until power is removed from the board. Switch S3-1 can be toggled as desired between ROM and RAM operation. In RAM mode, individual bytes of the program RAM can be modified via the debug software, if desired.

5.3. PC debug interface

Refer to the USB Development System Software Guide for information on operating in the PC debug mode.

5.4. I/O Port operation

On the development board, all I/O port bits (ports P0 to P3) operate identically, and are pseudo-bidirectional. As an output, each port bit provides a strong pull-down when a '0' is written to the bit. When a '1' is written to the port bit, it functions as a weak pull-up. The pull-up strength on the board is 5.6 kΩ (components RS2 & RS4 for port 0, RS5 & RS6 for port 1, RS7 & RS8 for port 2, and RS9 & RS10 for port 3). At all times, any read from an I/O port gives the digital value of the voltage on each pin. To configure any port bit as an input, a '1' must be written to that bit, and the input signal must be able to sink the pull-up current.

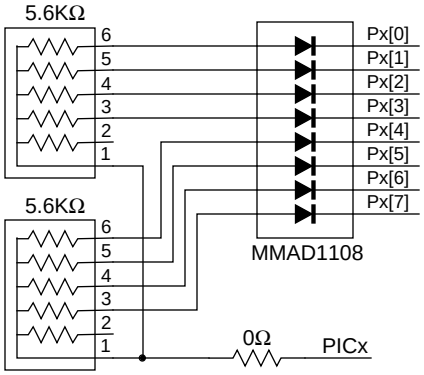


Figure 5. I/O Port Pull-Up Resistors

The I/O Port operation of the Cypress USB ICs differs from the operation of the development board. Figure 5.

shows the resistor pull-ups and diodes that are used with each GPIO port. The GPIO Configuration Register controls both the interrupt polarity and the driver mode. For both the IC and the development board the interrupt polarity works the same, but there are some differences in the driver mode. The CMOS mode on the IC is not available on the development board. The resistors for the resistive driver mode are located on the development boards as resistor packs RS1 through RS10.

After power up or manual reset, all I/O port bits have a '1' written to them, leaving them in the input/weak-pullup mode.

Each port is accessed by performing an I/O write or read operation to the appropriate address. All bits of the port are written or read together. Port addresses are given in the device specification.

5.5. Reset

Resets can be from one of these sources:

- Power on reset
- Watchdog reset (if enabled by switch S1-2; see Table 1)
- Pressing switch S2 generates a power on reset.

When one of these resets occur, the following actions take place:

- Program counter is reset to zero.
- Internal registers are reconfigured to their reset state (see device specification).

The contents of both the data RAM and the program RAM are undefined at power up, and are not affected by pressing the reset button.

5.6. USB Interface

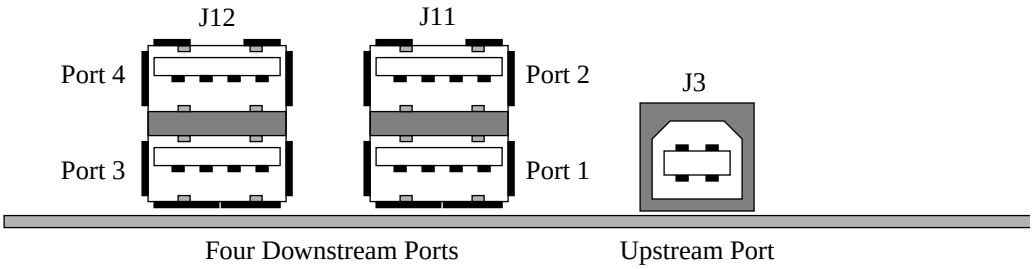
The upstream port on the development board supports the high speed (12.0 Mbps) USB mode. In this mode, the high-speed peripheral has a 1.5 kΩ pull-up to +3.3V on the D+ line. Resistor R34 provides this pull-up, and is included on the board (see Figure 4.). The board is shipped without a D- pull-up at resistor R33.

The four down-stream ports have two 15 kΩ resistors to ground.

Refer to the USB 1.0 specification for further details on the high speed USB mode.

For details on USB transmit and receive operation with the development board, consult the specification for the emulated Cypress USB device.

The following diagram shows the location of the four downstream ports:



6. Pin Descriptions

The development board contains three signal connectors: J2, a 60-pin header carrying target system signals; J1, a

60-pin header containing microcontroller interface signals (typically for logic analyzer connection); and J6, a 9-pin RS232 connector for communication with a PC. These are described in detail below.

6.1. Target Chip and Connector J2

Pin-outs for the CY7C65013 48-pin SSOP/PDIP and CY7C66013 56-pin SSOP configurations of the Cypress USB IC family are given in Table 3. Note that not all chip pins are implemented on the emulation board. All other pins on connector J2 are test points, ***and should not be connected to any other signal.***

Table 3: Target Chip Pins

Pin Name	CY7C64013 48-pin	CY7C65013 48-pin	CY7C66013 56-pin SSOP	Description	J2 Pin #
P0[0]		27	33	Port 0, Bit 0	2
P0[1]		22	24	Port 0, Bit 1	1
P0[2]		28	34	Port 0, Bit 2	4
P0[3]		21	23	Port 0, Bit 3	3
P0[4]		29	35	Port 0, Bit 4	6
P0[5]		20	22	Port 0, Bit 5	5
P0[6]		30	36	Port 0, Bit 6	8
P0[7]		19	21	Port 0, Bit 7	7
P1[0]		31	39	Port 1, Bit 0	10
P1[1]		18	18	Port 1, Bit 1	9
P1[2]		32	40	Port 1, Bit 2	12
P1[3]		17	17	Port 1, Bit 3	11
P1[4]		-	41	Port 1, Bit 4	14
P1[5]		-	16	Port 1, Bit 5	13
P1[6]		-	42	Port 1, Bit 6	16
P1[7]		-	15	Port 1, Bit 7	15
P2[0]		37	43	Port 2, Bit 0	18
P2[1]		12	14	Port 2, Bit 1	17
P2[2]		38	44	Port 2, Bit 2	20
P2[3]		11	13	Port 2, Bit 3	19
P2[4]		41	47	Port 2, Bit 4	22
P2[5]		8	10	Port 2, Bit 5	21
P2[6]		-	48	Port 2, Bit 6	24
P2[7]		7	9	Port 2, Bit 7	23
P3[0]		42	49	Port 3, Bit 0	26
P3[1]		-	8	Port 3, Bit 1	25
P3[2]		43	50	Port 3, Bit 2	28
P3[3]		6	7	Port 3, Bit 3	27
P3[4]		44	51	Port 3, Bit 4	30
P3[5]		-	6	Port 3, Bit 5	29
P3[6]		-	54	Port 3, Bit 6	32
P3[7]		-	-	Port 3, Bit 7	31
DAC[0]		-	31	DAC Port, Bit 0	34

Table 3: Target Chip Pins

Pin Name	CY7C64013 48-pin	CY7C65013 48-pin	CY7C66013 56-pin SSOP	Description	J2 Pin #
DAC[1]		-	26	DAC Port, Bit 1	33
DAC[2]		-	32	DAC Port, Bit 2	36
DAC[3]		-	25	DAC Port, Bit 3	35
DAC[4]		-	37	DAC Port, Bit 4	38
DAC[5]		-	20	DAC Port, Bit 5	37
DAC[6]		-	38	DAC Port, Bit 6	40
DAC[7]		-	19	DAC Port, Bit 7	39
D+[0]		1	1	Upstream Port 0, D+	42
D–[0]		2	2	Upstream Port 0, D–	41
VSS		24, 47	28, 55	Ground	43
				*	44
VPP		23	27	VPP	45
				*	46
				*	47
				*	48
				*	49
D+[1]		4	4	Downstream Port 1, D+	50
D–[1]		5	5	Downstream Port 1, D–	51
D+[2]		46	53	Downstream Port 2, D+	52
D–[2]		45	52	Downstream Port 2, D–	53
D+[3]		9	11	Downstream Port 3, D+	54
D–[3]		10	12	Downstream Port 3, D–	55
D+[4]		40	46	Downstream Port 4, D+	56
D–[4]		39	45	Downstream Port 4, D–	58
VCC		48	56	Positive Supply (+5V)	57**
VSS		24, 47	28, 55	Ground	59
VSS		24, 47	28, 55	Ground	60

* Not used on development system board

** Requires jumper JP1 to connect to +5V on the development system board (see Section 3.2)

6.2. J1 - Microcontroller Signals

For debug purposes, microcontroller interface signals are available at connector J1. Table 4 gives pin functions for the signals, and Table 5 lists all signal locations on the J1 connector. Consult Figure 4. for the correct position of pin 1.

Table 4: J1 Pin Descriptions

NAME	FUNCTION
PA[12:0]	13-bit address bus for program memory
ID[7:0]	8-bit Instruction Data from program memory
IROMS_	Program ROM chip select (active low)

Table 4: J1 Pin Descriptions

NAME	FUNCTION
SETUP	"OR" of SETUP (bit 7) in EPA0 & EPB0 Mode Registers
ITEN	Interrupt Enable
IRAMW_	Program RAM write enable (active low)
DA[7:0]	8-bit RAM Address bus
DB[7:0]	8-bit RAM Data bus
MR_	Memory read enable for data RAM (active low)
MW_	Memory write enable for data RAM (active low)
IOW_	I/O write enable (active low)
IOR_	I/O read enable (active low)
SOI	Start of instruction - goes high at beginning of new instruction
TRQ	Test Mode Request
IRQ	Interrupt Request Signal
IRA	Interrupt Acknowledge
BRA	Bus Request Acknowledge
BRQ	Bus Request - When high, data and address busses are driven externally
RESET	Reset signal for the board (active high)
RUN	Processor RUN
C12	12 MHz clock signal
VPP	EPROM Programming
VCC	Connection to development board's +5V
GND	Ground

Table 5: J1 Connector Pin-out

Pin #	Description	Pin #	Description
1	PA[0]	2	PA[1]
3	PA[2]	4	PA[3]
5	PA[4]	6	PA[5]
7	PA[6]	8	PA[7]
9	PA[8]	10	PA[9]
11	PA[10]	12	PA[11]
13	PA[12]	14	GND
15	SETUP	16	INTEN
17	IRAMW_	18	IOW_
19	IOR_	20	SOI
21	VPP	22	BRQ
23	IRQ	24	IRA
25	BRA	26	TRQ
27	RESET	28	RUN
29	MR_	30	MW_
31	GND	32	ID[0]
33	ID[1]	34	ID[2]
35	ID[3]	36	ID[4]
37	ID[5]	38	ID[6]
39	ID[7]	40	IROMS_
41	C12 (12 MHz)	42	GND
43	DB[7]	44	DB[6]
45	DB[5]	46	DB[4]
47	DB[3]	48	DB[2]
49	DB[1]	50	DB[0]
51	DA[7]	52	DA[6]
53	DA[5]	54	DA[4]
55	DA[3]	56	DA[2]
57	DA[1]	58	DA[0]
59	VCC	60	GND

6.3. J6 - RS232 Connector

J6 is a 9-pin female connector for RS-232 interface to a host PC. Connections are shown in Table 6. Pins not listed are not connected.

Table 6: J6 RS-232 Connector Pin-out

Pin	Function
2	RXD - Output data to PC
3	TXD - Input data from PC
5	Circuit Ground
6	DSR - RUN_ signal to PC debug interface
7	RTS - input from PC (not used)