

USB9603 Rev A1

User Product Information

National Semiconductor
September 2000
Revision 1.2



This document provides information on revision A1 of the National Semiconductor USB9603 chip.

This chip is available in two 28-pin packages: SOIC and CSP. The markings on line 2 of the respective package indicate the chip name; the markings on line 3 identify the chip revision.

Note that new information, added since the previous revision of this User Product Information, is marked with change bars.

Workarounds

Use the USB9604 device instead of the USB9603 for bus-powered applications.

The only difference between these two devices is the effect of a hardware reset on the clock generation circuit. In the USB9604, asserting the RESET input causes the clock generation circuit to be reset; in the USB9603, the clock generation circuit is not reset. For further details, refer to the USB9603/USB9604 datasheet.

1. CHIP

Revision A1 silicon has been analyzed and the following issues were found.

1.1 Voltage Regulator Output

The Voltage Regulator output value (pin V3.3) is slightly higher than the nominal voltage for default startup conditions. This same voltage is also fed to the USB transceivers.

Workaround

To obtain an accurate 3.3V value, write 0x40 to the Voltage Regulator Control Register, VREGCTL, at address 0x1f. (This is an internal test register, not documented in the datasheet.) All other values in this register should remain as is.

1.2 Stopping the Clock on XIN

If the clock on XIN is stopped when the USB9603 is not in HALT mode, the device locks up in an undefined state.

Workaround

Make sure that the device is in HALT mode before stopping the clock on XIN. For additional information, see the application note entitled "USB9603/4 Clock Stopping User Notes".

1.3 VBUS Brown-out after Warm Boot in Host PC

When a warm boot is performed in the host PC, the chipsets' USB hubs can create a brown-out on VBUS (VBUS voltage drops below the minimal voltage, approximately 1V, for a short period of time, approximately 20 msec).

This behavior is not defined in the USB specification, and falls under the inter-operability problem category.

Under these conditions, in a bus-powered application, USB9603 power-down sensing is not activated. In addition, the internal clock doubler that is reset by a power-up reset does not recover reliably, and the device can stop operating.



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