ALATEK AL8279
IP Core Application Note

December 10, 1999
(version 1.0)

General Information

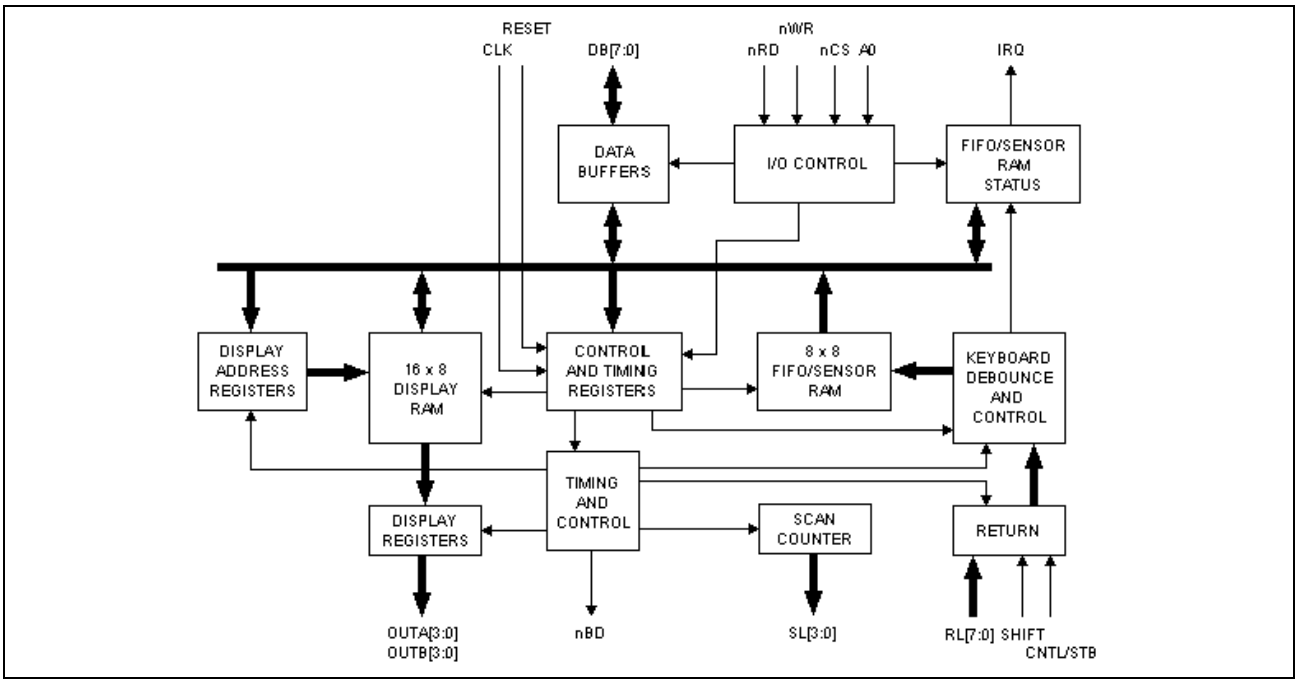
The AL8279 core is the VHDL model of the Intel™ 8279 Programmable Keyboard/Display Interface device designed for use with Intel microprocessors. The keyboard portion provides a scanned interface to 64-contact key matrix while the display portion provides an interface for popular display technologies (e.g. LED).

Features

- Functionally based on the Intel 8279 device
- Simultaneous keyboard display operations
- Scanned keyboard and sensor modes
- Strobed input entry mode
- 8-character keyboard FIFO
- 2-key lockout or N-key rollover with contact debounce
- Dual 8- or 16-numerical display
- Single 16-character display RAM
- Programmable scan timing and mode
- Interrupt output on key entry

Block Diagram

The basic structure of the AL8279 core is shown below:



Contents

A. Behavioral

The behavioral model is designed for the functional simulation only and it cannot be synthesized or implemented into FPGAs. The behavioral model contains the following files:

- **AL8279.vhd** - the top level of the AL8279 behavioral model

B. Synthesizable

See the Deliverables section of this document for further details.

C. Test Vectors

See the Deliverables section of this document for further details.

Interface

The pinout of the AL8279 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the table.

Signal Name	Signal Direction	Polarity	Description
DB[7:0] [1)]	INOUT	-	CPU data bus
CLK	IN	-	system clock
RESET	IN	HIGH	A high signal on this pin resets the device
CS	IN	HIGH	Chip Select
A0	IN	-	Buffer address
nRD, nWR	IN	LOW	Input/output read/write
IRQ	OUT	-	Interrupt request
SL[3:0]	OUT	-	Scan lines
RL[7:0]	IN	-	Return line
SHIFT	IN	-	Shift
CNTL/STB	IN	-	Control/Strobed Input mode
OUTA[3:0], OUTB[3:0]	OUT	-	Outputs
nBD	OUT	LOW	Blank display

NOTES:

1. Each bi-directional pin is defined in the core interface as three separated VHDL ports. Optionally, using the VHDL Interface (See the Deliverables section of this document for further details), it can be merged to one bi-directional VHDL port.

Implementation Data

The core has been synthesized and implemented to different types of reprogrammable devices. The model has been verified using the simulation environment and tested on the real hardware.

Software				
Synthesis Tool	Synopsys FPGA Express™ build 2.1.3.3220			
Implementation Tools	Xilinx Foundation™ 2.1i SP2, Altera MAX+plusII™ 9.21, Quartus™ 1.0 A			
Verification Tool	Active-HDL™ 3.5 build 437			
Hardware				
Vendor	**Xilinx**		**Altera**	
Device Family	4K	Virtex™	FLEX™ 10K	APEX™ 20K
Target Device	XC4062XLA-9	XCV300-4	EPF10K100-1	APEX20
Area*)	231CLBs (10%)	soon come	soon come	soon come
System Clock f_{max}	12MHz	soon come	soon come	soon come

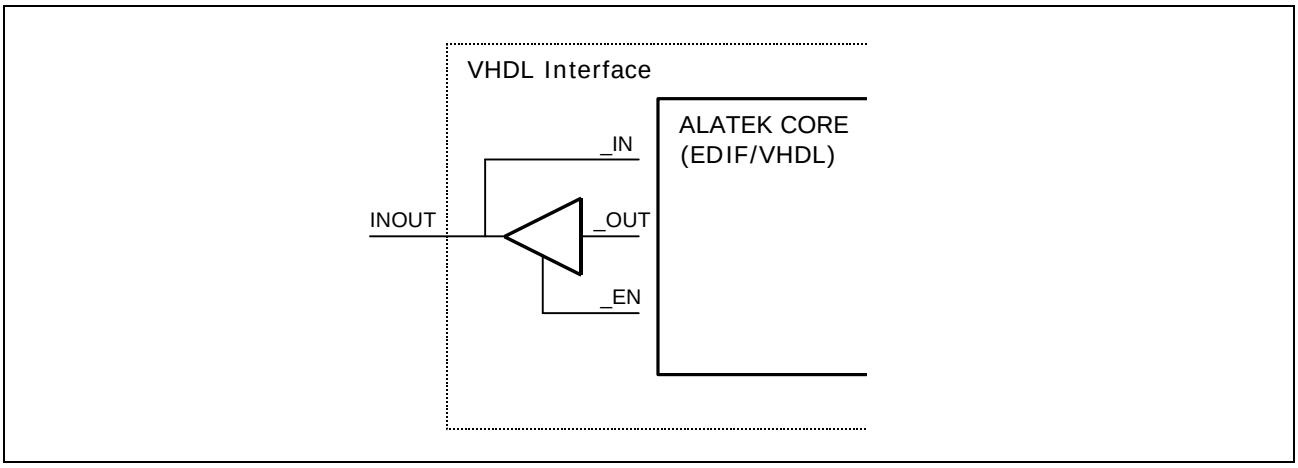
*) with RAM and ROM implemented

Deliverables

After you request the desired compiled synthesizable core, ALATEK delivers the following files:

- Both technology-dependent EDIF (AL8279_CORE.EDN) and VHDL (AL8279_CORE.VHD) netlists
- ALATEK VHDL Interface (AL8279.VHD)
- User-Guide and Application Notes
- Sample designs

Usually ALATEK delivers both EDIF and VHDL netlists for customers who order the synthesizable model. The EDIF netlist is used for the place and route process and VHDL is the post-synthesis netlist used for the simulation only. Of course, both netlists are technology-dependent, because they are created after the synthesis where the customer needs to specify a vendor, target family, etc.
ALATEK provides optionally a VHDL interface for its synthesizable models for these customers who need bi-directional ports in the core interface. See the picture below:



ALATEK can provide also a set of VHDL test benches for their cores. Usually they are sold at the additional charge.

Source codes are sold on a case-by-case basis.